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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUACH, TUAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/974,814	SAHARA ET AL.	
	Examiner	Art Unit	
	Tuan Quach	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *103,107,110,112-118,121,124,127,130,132-138 and 145-148* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1, 3-8, 10-15, 17-22, 24-29, 31-36, 38-43, 45-50, 52-57, 59-64, 66-103, 107, 110, 112-118,121, 124, 127, 130, 132-138, 145-148
Continuation of Disposition of Claims: Claims withdrawn from consideration are 1,3-8,10-15,17-22,24-29,31-36,38-43,45-50,52-57,59-64 and 66-102.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 20, 2005 has been entered.

Claim 121 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

This claim depends from cancelled claim 120.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 103, 107, 110, 112-116, 133, 136 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 325 328, Kamal, Hong, Lee, and Zeininger taken together, and further in view of Huang of record.

Re claim 103, 107, 110, 112-116, 133, 136, '328 teaches forming semiconductor integrated circuit device comprising forming a gate insulating film on semiconductor substrate 1, forming conductive gate 6, 7, forming self-aligned lightly doped semiconductor regions 12/13, forming second insulating films 14 on side surface of conductive or gate 6, 7, forming second semiconductor region 10 and 11 of source/drain regions having higher concentration , HF cleaning, argon sputter etching of less than 20 nm, including conformal cleaning thus of the gate surface as well, and encompassing less than 2.5 nm, forming silicides 6a-11a, including cobalt silicide. See column 6 line 1 to column 7 line 45, column 14 line 40. '328 lacks anticipation in that it does not explicitly recite the gate dimension to be of 0.18 micron or less, and does not recite the isolating element, the conductive film on such isolating element.

Such selection of gate dimension nonetheless would have been encompassed in such processing given that such processing does not preclude or exclude its application to form devices of desired structures, including devices wherein the gate is less than 0.18 micron. In any event, the application of the same processing into device structures having reduced dimensions does not require any inventiveness and does not impart any patentabilibity into the conventional processing taught by '328.

Hong also teaches self-aligned silicidation process including sub-0.18 micron CMPS wherein prior to silicidation, the use of argon sputter clean is taught wherein leakage can be reduced and application to submicron device is realized. The process allows low diode leakage silicidation and application to sub-0.18 micron NMOS technology. See page 107-108, Figs. 1-17.

Kamal also teaches self-aligned silicidation including forming gate 202, lightly doped regions aligned to gate, source drain 208, aligned to spacer 210, the sputter etching prior to metal deposition and silicidation. See column 2 lines 1 to column 3 line 23, column 3 line 65 to column 10 line 19. The contemplation to sub-0.18 micron dimension is also encompassed and contemplated (column 2 line 2. Kamal further shows the extent of the etching including the selection of removal of 20 angstrom, column 5 line 65. The advantages of silicide contacts upon such sputter cleaning including self-aligned contacts having improved device characteristics. See column 2 line 48 to column 7 line 48.

Lee teaches application of semiconductor device having reduced performance, e.g., 0.13 micron CMOS process where gate length or width of below 0.13 micron is employed to improve circuit performance and increase packing density. The use of gate, LDD implant, insulating spacer, source drain implant, and cobalt salicidation is also taught. See page 136-137, table 1.

Zeininger teaches the formation of cobalt silicide contacts to device regions of deep-submicron including sputter etching between 3 and 20 mono layers to remove the native oxide, wherein an ultra shallow damage region would be achieved prior to

forming cobalt silicide contacts. Appropriate cobalt silicide thickness such as 300 nm or less is also shown. See column 2 line 25 to column 3 line 38.

It would have been obvious to one skilled in the art in practicing the above process to have applied such process into making submicron device since such application is conventional and obvious as evidenced by Hong or Lee wherein devices of reduced dimensions and improved characteristics can be obtained. Conversely, although Hong or Kamal do not the details of forming the LDD region, spacer, and source, drain, such provision in Hong or Kmal would have been conventional and obvious wherein device components such as LDD, spacer, and source drain can be obtained as taught by "328 or Lee. Note that the positioning as now claimed to the cobalt silicide positioned such that current leakage is prevented, e.g., claim 103 last five lines, would have been obvious given the silicide structures as shown and the same advantage regarding leakage is taught, as apparent in '328, Hong, page 107, and furthermore, as the "wherein" and/or "whereby" recitation does not add any additional limitation regarding processing involved and merely states the result of the limitations in the claim thus adds nothing to the patentability or substance of the claim. See *Texas Instruments Inc. v. International Trade Commission*, 26 USPQ2d 1010 (Fed. Cir. 1993); *Griffin v. Bertinia,* 62 USPQ2d 1431 (Fed. Cir. 2002); *Amazon.com Inc. v. Barnesandnoble.com Inc.*, 57 USPQ2d 1747 (Fed. Cir. 2001). Furthermore, the prior art solves the same problem of leakage current evidencing that such leakage is prevented and that the contacts through the junctions do not result therefrom. The silicide contacts to the second regions and not to the first regions would have been

apparent in '328 at the portions delineated above, and as shown in Kamal Fig. 10, wherein the exposed region contact to the second regions and not the first region which is blocked by the spacers. The associated reduced leakage current would be obtained as the sputter etching including the ultra shallow is taught as delineated above and is readily apparent in Hong.

The removal of 2.5 nm or less of the top of the semiconductor substrate would have been met in '328 or Hong above and furthermore would have been a matter of optimization to remove the desired native oxide as evidenced by Kamal, as delineated above, e.g., 20 angstroms. Accordingly, it would have been obvious to one skilled in the art to have employed the shallow removal range of the sputter etching including within the range of 25 nm or less since such would have been encompassed in '328 and Hong and further corresponds to an optimization well within the purview of one skilled in the art including a conventional removal range amply delineated in Kamal and in Zeininger wherein the removal of as low as a few monolayers (between 3 and 20 monolayers) can be effected to effect an ultrashallow region prior to formation of the silicide contact to improve device characteristics.

Regarding the provision of the isolating element, such would have been obvious as shown in Huang, 6,117,723, column 3 lines 22, isolation region 2, including formation by thermally grown or insulator filled for isolating active regions, including the provision of the gate or conductive film on such element, column 3 lines 53-59, structure 7b, 7c, Fig. 3, column 5 lines 11. Regarding the formation of the islation region by forming trench and filling with insulator as in claim 133, such trench isolation by filling a trench

with insulator is well known as evidenced by Huang above. Regarding claim 136, the height of steps is not sufficiently defined as to how such are formed as well as the extent of the steps or how much is reduced and in any event would appear to have followed since the sputter etching is normally effected in a blanket fashion, including the gate as well as the regions of the substrate and thus any height reduced by such cleaning would inherently follow, given that the sputter etching employed by applicant is effected in the same manner taught in the prior art.

Regarding claim 107, the use of HF cleaning is well known in the art as evidenced by '328 as delineated above wherein cleaning can be effected. Regarding claim 108, the use of Ar sputter etching is well known in the art and is amply shown above. The use of cobalt for cobalt silicidation is well known in the art and is amply shown above. Regarding claim 110, the cobalt silicide thickness being between 200 and 400 angstrom would have been a matter of routine optimization and well known in the art and is amply shown above, including by Zeininger as delineated. Regarding claim 112, the removal of the top of the conductive film and/or of the semiconductor device would correspond to the sputter etching including of the gate and/or source drain region where the silicide contacts are desired as shown above. Regarding claims 113-116, the recessed region claimed would correspond to the corresponding regions in the prior art upon which the sputter etching is applied in the same process as in the instant application and would have been obvious for the reasons delineated above and as discussed above wherein the sputter etching is effected in a blanket fashion and would effect the gate as well as the source/drain regions.

Claims 117, 118, 121, 124, 127, 130, 132, 134, 135, 137, 138, 145-148 are rejected under 35 U.S.C. 103(a) as being unpatentable over 328, Kamal, Hong , Lee, Zeininger, and Huang, as applied to claims above, and further in view of Rho or Yan.

Regarding claims 117 and 118, including the selection of the first doped regions to be less than 50 nm and second regions to be less than 1500 angstroms, such optimization to obtain submicron device would have been encompassed in the prior art above which does not preclude or exclude such junction depths. Furthermore, Rho shows that it is important to form extremely shallow source/drain junction to reduce short channel effect in submicron devices. See page 291, 292, Fig. 4. Yan also shows the conventionality of shallow junctions, e.g., Fig. 2, pages 86 and junction depth of 300 angstroms and its application to submicron devices having high performance good subthreshold characteristics and controlled short channel effects.

It would have been obvious to one skilled in the art to have optimized the doped region thicknesses as such would have been encompassed in the references delineated above which do not preclude such range, e.g., Hong, to obtain shallow junctions, Fig. 3, 5, 9, and as shown in Rho or Yan above wherein such optimization would allow formation of shallow source drain junctions and permit reduction of short channel effects and applications in deep submicron devices.

The thickness of cobalt silicide being 20 to 40 nm, the sputter etch being 2.5 nm is less for the top of the conductive gate and simultaneous sputter etching in claims 121, such correspond to the similar limitations previously discussed in claims 110, 112, 113, above and would have been obvious for the reasons delineated above and as

discussed above wherein the sputter etching is effected in a blanket fashion and would effect the gate as well as the source/drain regions

Regarding claims 124 and 127, this corresponds to substantially similar limitations in claim 103 and 117 or 118, with the components of the FET devices now being specifically called, e.g., a MISFET instead of a semiconductor device, gate instead of a conductive film in claim 103, first source/drain aligned with the gate instead of first semiconductor regions, sidewall of MISFET instead of insulating film on side surface of conductive film, etc., nonetheless correspond to substantially same subject matter render obvious by the teachings delineated above with regard to claim 103, 117 and 118 above. The limitation of first source drain to be 50 nm in claim 124 step d) and second source drain to be less than 50 nm or less as in claim 127 step d) correspond to the limitations in claim 117 and 118, and the thickness as in claims 145 and 146 and accordingly, such would have been further obvious for the same reasons delineated above wherein such shallow junctions are not precluded or excluded by the applied prior art and wherein such shallow junctions are explicitly recited to be advantageous to obtain reduced short channel effects in deep submicron applications as delineated in Rho or Yan.

Regarding claims 130, 132 concerning cobalt thickness of 20 to 40 nm, sputter etch also of the gate and simultaneous, such correspond to the limitations in claims 112, 113, above and as discussed above wherein the sputter etching is effected in a blanket fashion and would effect the gate as well as the source/drain regions. Regarding claims

133-135, the isolating region by filling trench with insulating film is notoriously conventional as taught in Huang as discussed above.

Regarding claims 136-138 and 147-148, the wherein limitation appears to recite a result as opposed to any additional processing and such does not impart patentability as delineated above wherein in any event would appear to have followed since the same processing is employed in the prior art, namely the sputter etching is normally effected in a blanket fashion, including the gate as well as the regions of the substrate and thus any height reduced by such cleaning would inherently follow, given that the sputter etching employed by applicant is effected in the same manner taught in the prior art. Thus, to the extent that such step is created or reduced in association with or incidental during the isolating element formation, then the reduction of the step would appear to follow as well since the sputter cleaning applied by applicant would appear to apply in the same manner in the prior art as delineated above. Similarly, the wherein recitation regarding uniform or or even silicide as in claims 147 and 148 would be unpatentable over the prior art as there is no additional processing involved and wherein such would follow from the prior art employing the same process taught by applicant.

Applicant's arguments with respect to the pending claims above have been considered but are moot in view of the new ground(s) of rejection.

As delineated above, regarding the amended limitations regarding Ar for the sputter etching and of cobalt as the metal for silicide contacts, such correspond to the

notoriously conventional Ar sputter etching and of conventional silicide contacts as amply demonstrated in the prior art above.

In sofar as applicable, regarding the associated issue of isolating region, step height, etc., in the amended portions or new claims, see the new ground of rejections delineated above. In any event, in the absence of specific and positive processing and wherein the instant invention employs the same blanket sputter cleaning as in the prior art including using the same processing in the prior art for forming the isolation regions, it remains that the reduction of height, to the extent such can be determined from the claims would follow from the application of the prior art processing as delineated above.

Regarding applicant's argument that all the limitations taught by the prior art. See the new grounds above discussing the amended limitations as well. Applicant point out that the critical value and advantages are obtained when the etching is within certain ranges, e.g., less than 1 or 2 nm, as delineated in Fig. 9 and [0050]. Such has been carefully considered but it remains that the various advantages are taught by the prior art as delineated above and wherein the prior art employs similar amount of etchings. The comparison is made when the sputter etching is not carried out, e.g., [0050], while in the prior art, such is carried out, and including etching less than 2.5 nm, in the same range taught by applicant.

Regarding the argument that when the sputter etching is greater than 2.5 nm, then current leakage increased. This has been carefully considered together with Fig. 15. It would appear nonetheless that such increased in current leakage would be expected given the depth of the associated junction. Additionally, such reduced

leakage current also is taught in the prior art, including Hong which also teaches self-aligned silicidation process including sub-0.18 micron CMPS wherein prior to silicidation, the use of argon sputter clean is taught wherein leakage can be reduced and application to submicron device is realized. The process allows low diode leakage silicidation and application to sub-0.18 micron NMOS technology. In addition, as delineated above, the removal of 2.5 nm or less of the top of the semiconductor substrate would have been met in '328 or Hong above and furthermore would have been a matter of optimization to remove the desired native oxide as evidenced by Kamal, as delineated above, e.g., 20 angstroms. Accordingly, applicant's advantage in selecting the range of 2.5 nm has been carefully considered but it remains obvious to one skilled in the art to have employed the shallow removal range of the sputter etching including within the range of 25 nm or less since such would have been encompassed in '328 and Hong and further corresponds to an optimization well within the purview of one skilled in the art including a conventional removal range amply delineated in Kamal and in Zeininger wherein the removal of as low as a few monolayers (between 3 and 20 monolayers) can be effected wherein an ultrashallow region can be obtained prior to formation of the silicide contact to improve device characteristics.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Quach
Primary Examiner